REMARKS

The non-final office action of August 30, 2007, has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-2, 4, and 35-38 have been amended to place the claims in a more preferred form. Claims 16-34 have been canceled without prejudice or disclaimer. New claim 39 has been added. Claims 1-15 and 35-39 remain in this application.

Claims 2 and 4 stand objected to due to informalities. Specifically, the Action requests that regarding claim 2, "configuration bit look-up table" should be changed to "the configuration bit look-up table," and regarding claim 4 the Action requests that "multiplexor" should be spelled "multiplexer." Claims 2 and 4 have been amended accordingly.

Claims 1-15 and 35-38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,706,216 to Carter (hereinafter referred to as "*Carter*"). Applicants respectfully traverse.

The Action alleges that *Carter* discloses all the features of claim 1. The Action points to combinational logic 100 to show data processing portion, storage circuit 120 to show storage unit and select logic 110 and 111 to show configuration bit look-up table (Action, p. 3). The cited portion of *Carter* (Fig. 7; col. 9, lines 51-63; Fig. 8; col. 9, lines 21-24) fails to disclose all of the recited features of claim 1. The cited portions of *Carter* describe a configurable combinational logic element 100 (the alleged data processing portion), which includes configurable switches, 8-bit RAMs, select logics 110 and 111 (the alleged configuration bit look-up table), multiplexer and switches. The select logics 110 and 111 select a unique storage element in a RAM for each of possible combinations of binary signals, and the multiplexer provides an output signal from either of the select logics 110 and 111.

Amended claim 1 recites, among other features, "wherein the data processing portion is configured to extract a set of bits for a single output from the configuration bit look-up table." Applicants submit that *Carter* fails to disclose at least these features of claim 1. Even assuming, without admitting, that the select logics 110 and 111 in *Carter* are look-up tables or that the bits stored in the RAM are look-up tables, *Carter* fails to disclose or even suggest that the data processing portion extracts a set of bits for a single output from the look-up table. Rather, in

Carter (per the cited col. 9, lines 21-24), the select 110 outputs just one bit for each of eight possible combinations of signals A, C, and D, from an eight bit RAM. *Carter* also describes in col. 9, lines 24-25, that select logic 111 operates similarly. As such, the cited portions *Carter* fail to disclose the above recited features of amended claim 1. In addition, no other portion of *Carter* teaches or suggests these features.

Therefore, amended claim 1 is patentable over *Carter*, and claims 2-15, which depend from claim 1, are patentably distinct from *Carter* for at least the same reasons as their ultimate base claim and further in view of additional advantageous features recited therein.

The Action alleges that *Carter* discloses all the features of claims 35 and 36. Amended claims 35 and 36 recite similar features as described above with respect to Applicants' claim 1. Therefore, for at least similar reasons as discussed with respect to claim 1 above, claims 35 and 36 are patentable over *Carter*.

The Action alleges that *Carter* discloses all the features of applicants' claim 37. Amended claim 37 calls for, among other features, "the configuration bit look-up table including a matrix of zeros and ones, with the ones along one diagonal." Applicants submit that *Carter* fails to teach at least these features of claim 37.

Carter is wholly devoid of any teaching or suggestion of the above recited features of amended claim 37. In particular, claim 37 fails to disclose or even suggest that the bit look-up table includes a matrix of zeros and ones with the ones along one diagonal of the matrix. At best, *Carter* describes a "Karnough" map representing an output signal for a number of possible combinations of input signals. For example, in col. 4 lines 37-66 of *Carter*, even assuming, without admitting, that the "Karnough" map for the 16 RAM is a look-up table, the "Karnough" map does not disclose or suggest that the bit look-up table includes a matrix of zeros with ones along one diagonal. In fact, *Carter* describes that "[s]hould a binary "1" be desired both when A=0, B=0, C=0 and D=0 and also when A=1, B=0, C=0 and D=0 then a binary "1" is stored at each of the intersections of the first column with the first row and the second row." (*Carter* col. 4, lines 59-63). Notably, this construction will not have ones along one diagonal, because there will be two "1" bits in the first column.

Therefore, in view of the above, neither the cited portion of *Carter* nor any other portion of *Carter* discloses or suggests the recited features of amended claim 37 above. Amended claim 38 recites similar features as described above with respect to Applicants' claim 37. Therefore, for at least similar reasons as discussed with respect to claim 37 above, claim 38 is patentable over *Carter*.

New claim 39 is fully supported by the original specification and believed allowable over the art of record.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the examiner is requested to contact the undersigned at (202) 824-3155.

Respectfully submitted,

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